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PATENT NUMBER

U.S. **UTILITY** Patent Application

O.I.P.E. PATENT DATE

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APPLICATION NO. 09/850228	CONT/PRIOR F	CLASS	SUBCLASS 503	2 1:8:4	EXAMINER / e.c.
Satoru Ki	shimoto		1	2162	PATEL

Placement and routing method for clock distribution circuit, clock distribution circuit manufacturing method, semiconductor device manufacturing method, clock distribution circuit and semiconductor device PTO-2040
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